

CLAIMS

1. A stacked microelectronic assembly comprising:
a continuous sheet having oppositely-directed obverse and reverse surfaces, the sheet including a core panel having edges, the sheet further including at least two side panels, each of the side panels having a folded portion connecting that side panel to the core panel along one of the edges so that when folded to form a stack with the core panel the at least two side panels are substantially aligned in a plane substantially parallel to the core panel;
microelectronic elements mounted on at least two of the panels;
terminals on the sheet; and
one or more wiring layers including traces extending along the sheet between the panels by way of the folded portions, at least some of the traces connecting the microelectronic elements to at least some of the terminals.
2. An assembly as claimed in claim 1, wherein the core panel is disposed at the top or bottom of the stack, the terminals are disposed on the core panel and exposed for connection to an external circuit, the microelectronic elements including at least two microelectronic elements, each mounted on the at least two side panels.
3. An assembly as claimed in claim 2, wherein the traces connecting a first one of the microelectronic elements mounted on a first one of the side panels to the terminals on the core panel are of substantially equal length to traces connecting a second one of the microelectronic elements mounted on a second one of the side panels to the terminals on the core panel.
4. An assembly as claimed in claim 3, wherein the first and second microelectronic elements are substantially identical to one another.
5. An assembly as claimed in claim 4, wherein the first and second microelectronic elements are memory chips.

6. An assembly as claimed in claim 5, wherein each memory chip includes at least one chip select contact and a plurality of common contacts, and wherein the terminals include a plurality of common terminals and a plurality of chip select terminals, the traces including chip select traces connecting each of the chip select terminals to a chip select contact of only one of the chips and common traces connecting each the common terminal to common contacts of the first and second chips.

7. An assembly as claimed in claim 2, wherein the terminals on the core panel are movable with respect to the microelectronic elements mounted on the side panels.

8. An assembly as claimed in claim 7, wherein the folded portions of the sheet and at least those portions of the traces extending along the folded portions are flexible.

9. An assembly as claimed in claim 2, wherein the core panel is generally rectangular and the edges include first and second edges, the at least two side panels including first and second side panels connected to the first and second edges, respectively, of the core panel, and wherein the microelectronic elements include first and second microelectronic elements mounted on the first and second side panels, respectively.

10. An assembly as claimed in claim 9, wherein the first and second edges are opposite each other.

11. An assembly as claimed in claim 9, wherein the traces include first and second sets of traces connecting the first and second microelectronic elements, respectively, to the terminals and wherein the traces of each set have substantially the same length as traces in every other one of the sets.

12. An assembly as claimed in claim 1, wherein the terminals are disposed on the core panel and the microelectronic elements include a core panel chip mounted to the core panel and connected to at least some of the terminals

and at least two side panel chips mounted on the side panels and connected to the core panel chip through the traces.

13. An assembly as claimed in claim 12, wherein the terminals on the core panel are movable with respect to the core panel chip.

14. An assembly as claimed in claim 13, wherein a compliant layer is provided between the core panel and the core panel chip.

15. An assembly as claimed in claim 12, wherein the side panel chips are memory chips.

16. An assembly as claimed in claim 1, wherein the at least two side panels are disposed at the top or bottom of the stack, the terminals are disposed on the side panels and exposed for connection to an external circuit.

17. A microelectronic package comprising an elongated substrate having a first side panel, a second side panel and a core panel disposed between the first and second side panels, and a microelectronic device mounted to one of the panels, the substrate being folded so that the first panel and the second panel overlie the core panel with the microelectronic device disposed between the core panel and at least one of the first and second side panels, the substrate having a first set of traces extending along the substrate from the core panel to the first side panel and a second set of traces extending along the substrate from the core panel to the second side panel;

wherein the substrate has a set of core terminals disposed on the core panel, a first set of terminals disposed on the first side panel and a second set of terminals disposed on the second side panel, the first set of terminals and the second set of terminals defining a common array on one side of the folded substrate.

18. A package as claimed in claim 17, wherein the first side panel is connected to the core panel via a first edge and the second side panel is connected to the core panel via a

second edge, and wherein the first edge and the second edge are opposite each other.

19. A package as claimed in claim 17, wherein the microelectronic device is a processor mounted on the core panel and memory devices are mounted are the first and second side panels and wherein the processor is electrically coupled to the memory devices via the first and second set of traces.

20. A microelectronic package comprising an elongated substrate having a first side panel, a second side panel and a core panel disposed between the first and second side panels, and a microelectronic device mounted to one of the panels, the substrate being folded so that the first panel and the second panel form a common array over the core panel, the substrate having a first set of traces extending along the substrate from the core panel to the first side panel and a second set of traces extending along the substrate from the core panel to the second side panel and wherein the microelectronic device is coupled to at least one of the first and second set of traces.

21. A package as claimed in claim 20, wherein the first side panel is connected to the core panel via a first edge and the second side panel is connected to the core panel via a second edge, and wherein the first edge and the second edge are opposite each other.

22. A package as claimed in claim 20, wherein the microelectronic device is a processor mounted on the core panel and memory devices are mounted are the first and second side panels and wherein the processor is electrically coupled to the memory devices via the first and second set of traces.

23. A stacked microelectronic assembly comprising:

a continuous sheet having oppositely-directed obverse and reverse surfaces, the sheet including a core panel having edges, the sheet further including at least two side panels, each of the side panels having a folded portion connecting that side panel to the core panel along one of the edges;

a first microelectronic element mounted on a first one of the at least two of the panels;

a second microelectronic element mounted on a second one of the at least two of the panels;

a third microelectronic element mounted on the core panel;

terminals on the sheet; and

one or more wiring layers including traces extending along the sheet between the panels by way of the folded portions, at least some of the traces connecting the microelectronic elements to at least some of the terminals;

wherein, sides of the first microelectronic element and the second electronic element face each other.

24. An assembly as claimed in claim 23, wherein the first and second microelectronic elements are memories and the third microelectronic element is a processor.

25. An assembly as claimed in claim 23, wherein the at least two side panels include a first side panel connected to the core panel via a first edge and a second side panel connected to the core panel via a second edge such that the first edge and the second edge are opposite each other.

26. A method of making a stacked electronic assembly comprising:

a) providing a substrate in the form of a flat sheet having a first surface and a second surface opposite the first surface, a plurality of electrically conductive terminals accessible at one of the first and second surfaces of the substrate, a wiring layer, the sheet including a core panel having edges and a plurality of side panels projecting from the edges of the core panel, the wiring layer comprising traces extending along the sheet from the core panel to the side panels and being electrically connected to the terminals;

b) assembling a plurality of microelectronic elements to the panels for electrically connecting the microelectronic elements to the traces; and

c) folding portions of the side panels about a plurality of fold axes adjacent the edges of the core panel so as to stack at least some of the microelectronic elements such that at least two of the microelectronic elements from different side panels substantially lie in a common plane substantially parallel to the core panel.

27. A method as claimed in claim 26, wherein the terminals are disposed on the core panel, the folding comprising folding the portions of the side panels so that the terminals are exposed for connection to an external circuit.

28. A method as claimed in claim 26, wherein at least the portions of the side panels and at least those portions of the traces extending along the portions of the side panels are flexible.

29. A method as claimed in claim 26, wherein the panels have first and second surfaces, the first and second surfaces of the panels being portions of the first and second surfaces of the substrate, respectively, the folding being performed so that the first surface of at least one of the side panels faces the first surface of the core panel and the first surface of at least one other of the side panels also faces the first surface of the core panel.

30. A method as claimed in claim 29, wherein the terminals are disposed on one of the side panels, the folding comprising folding the portions of the side panels so that the terminals are exposed for connection to an external circuit.

31. A method of making a stacked electronic assembly comprising:

a) providing a substrate in the form of a flat sheet having a first surface and a second surface opposite the first surface, a plurality of electrically conductive terminals accessible at one of the first and second surfaces of the substrate, a wiring layer, the sheet including a core panel having edges and a plurality of side panels projecting from the edges of the core panel, the wiring layer comprising

traces extending along the sheet from the core panel to the side panels and being electrically connected to the terminals;

b) assembling a plurality of microelectronic elements to the panels for electrically connecting the microelectronic elements to the traces;

c) testing at least some of the microelectronic elements to determine failures thereof;

d) disabling those side panels holding failed microelectronic elements; and

e) folding portions of the side panels attached to the core panel about a plurality of fold axes adjacent the edges of the core panel so as to stack at least some of the microelectronic elements.

32. A method as claimed in claim 31, wherein the disabling step includes the step of cutting-off those side panels holding failed microelectronic elements.

33. A method as claimed in claim 31, wherein the disabling step includes the step of electrically disconnecting the failed microelectronic elements from traces coupled thereto.

34. A method of making a stacked electronic assembly comprising

a) providing a substrate in the form of a flat sheet having a first surface and a second surface opposite the first surface, a plurality of electrically conductive terminals accessible at one of the first and second surfaces of the substrate, a wiring layer, the sheet including a core panel having edges and a plurality of side panels projecting from the edges of the core panel, the wiring layer comprising traces extending along the sheet from the core panel to the side panels and being electrically connected to the terminals;

b) assembling a plurality of microelectronic elements to the panels for electrically connecting the microelectronic elements to the traces;

c) testing at least some of the microelectronic elements to determine failures thereof;

d) identifying those microelectronic elements assembled on side panels that have failed;

e) determining from the identified failed microelectronic elements if an operational, reduced functionality and/or capacity, stacked electronic assembly is possible notwithstanding the identified failed microelectronic elements;

f) if an operational stacked electronic assembly is possible, disabling those side panels having failed microelectronic components; and

g) folding portions of the side panels about a plurality of fold axes adjacent the edges of the core panel so as to stack at least some of the microelectronic elements.

35. A method as claimed in claim 34, wherein the disabling step includes the step of cutting-off those side panels holding failed microelectronic elements.

36. A method as claimed in claim 34, wherein the disabling step includes the step of electrically disconnecting the failed microelectronic elements from traces coupled thereto.

37. A method as claimed in claim 34, wherein the determining step includes the step of referencing data defining possible operational combinations of the plurality of microelectronic elements.

38. A method as claimed in claim 34, wherein the capacity relates to a memory capacity of the stacked electronic assembly.

39. A method as claimed in claim 38, wherein the assembling step includes the step of mounting memory devices on the plurality of side panels.

40. A method as claimed in claim 39, wherein the assembling step mounts one memory device on each of the plurality of side panels.